Active-HDL™ FPGA Design and Simulation

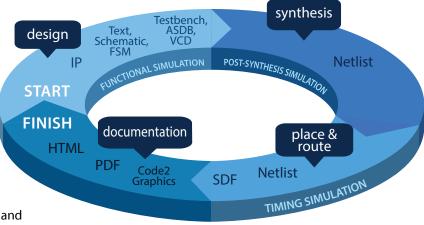
Design Creation and Simulation

Active-HDL™ is a Windows® based, integrated FPGA Design Creation and Simulation solution for team-based environments. The Integrated Design Environment (IDE) within Active-HDL includes a full HDL and graphical design tool suite and RTL/gate-level mixed language simulator for rapid deployment and verification of FPGA designs.

The design flow manager evokes over 200 EDA and FPGA tools, during design entry, simulation, synthesis and implementation flows and allows teams to remain within one common platform during the entire FPGA development process. Active-HDL supports industry leading FPGA devices from Intel (Altera)®, Lattice®, Microsemi™ (Actel), Quicklogic®, Xilinx® and more.

Top Benefits

- **Unified Team-based Design Management**
- Deploy designs quickly with Text, Schematic and **State Machine**
- Powerful common kernel mixed-language simulator (VHDL, Verilog, SystemVerilog/UVM, and SystemC)
- Advanced Debugging and Code Coverage
- Assertion-Based Verification (SVA, PSL, OVA)
- DSP Co-simulation with MATLAB®/Simulink® interface
- Share designs quickly with auto-generate Design **Documentation in HTML and PDF**



Design

The Design Suite within Active-HDL utilizes graphical and textual design entry methods, and integrates over 200 EDA tools into a single platform. Design management tools help eliminate issues faced by team-based designs during the FPGA developement process.

Debug

Active-HDL incorporates a common kernel mixed-language simulator with interactive tools that enables designers to debug quickly. Debugging tools such as Advanced Data Flow and Xtrace provide users a graphical representation of the system's internal signals increasing observability and aiding in the debug of large designs. Active-HDL also includes Code Coverage and Analysis tools, allowing designers to incorporate metric-driven verification into the design process.

Document

Active-HDL allows designers to quickly document all aspects of their design workspace for later review, reuse, and archiving. This enables the ability to maintain proper documentation at all stages of the development process, eliminating many issues faced by multi-team design environments.



STANDARDS -















SILICON











- INTERFACES —





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SYNOPSYS°



FEATURES PRODUCT CONFIGURATIONS

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