Sigasi;

Deal with the complexity of VHDL, Verilog, SystemVerilog and Mixed Languages

# **Sigasi Studio** is an intelligent hardware design tool that features advanced programming assistance for digital hardware engineering

## HARDWARE DESIGN MADE FASTER, EASIER AND MORE EFFICIENT

HDL (VHDL/Verilog/SystemVerilog) design is difficult and complex. That's why we created Sigasi Studio as a design creation tool that deals with that complexity. Sigasi Studio makes your hardware design:

**Faster_** Our secret ingredient is the super fast built-in compiler. Because Sigasi Studio understands your code while you type, we can help you be more productive, produce higher quality work and excel in your work.

**Easier_** A basic text editor just won't do if you want to write code like a pro. Sigasi Studio is an intelligent design tool that offers advanced design assistance. Why walk if you can drive... or get driven to your destination?

**More efficient_** Sigasi Studio guides you through complex code designs. With instant feedback on errors and auto-completion suggestions. Reducing development time and helping you and your team write better code.

## SAVE TIME AND MONEY

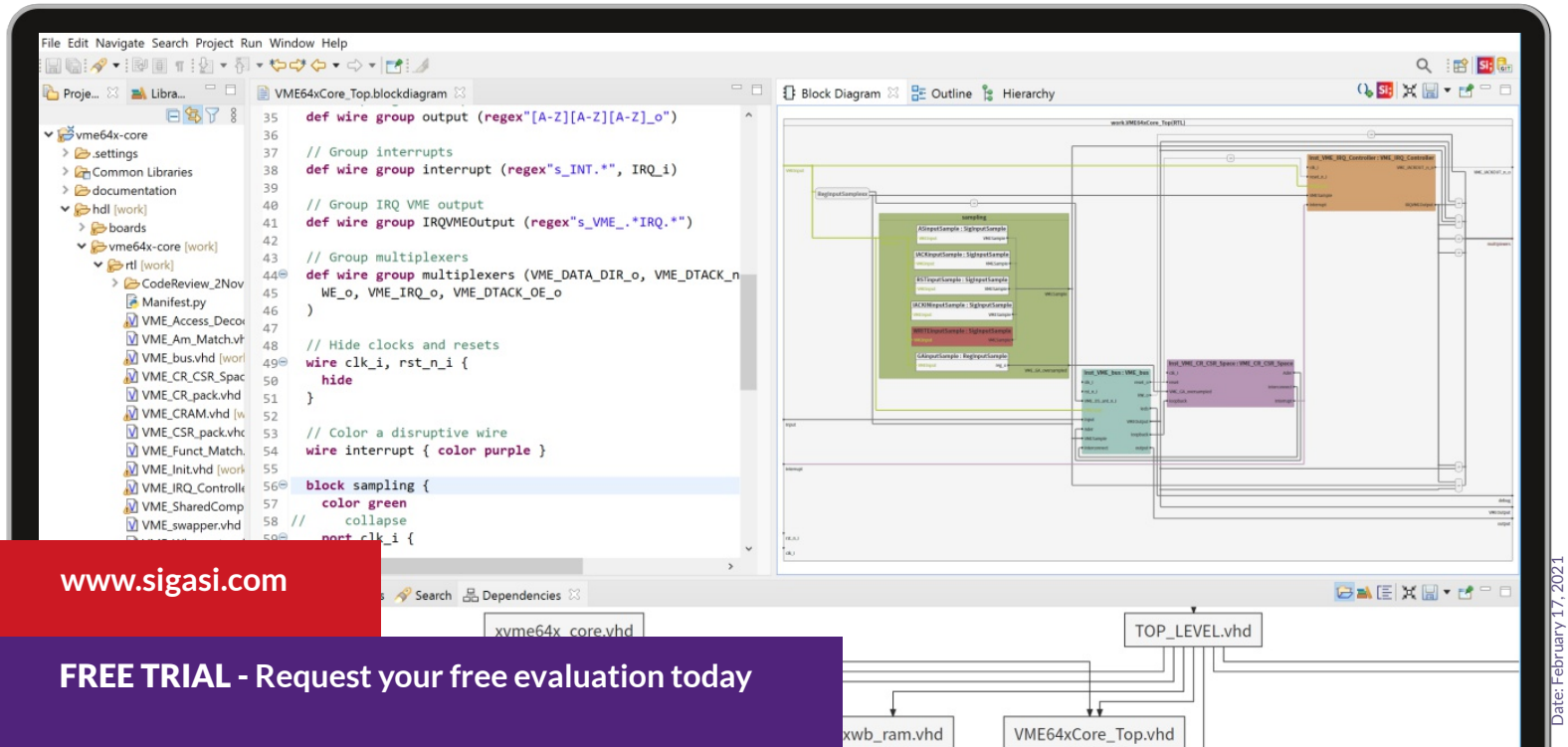
Sigasi Studio is your personal assistant, it provides you with:

**Code editing_** Intelligent content assist makes it easy to create perfect HDL code. Existing design elements and keywords are completed based on the context, and adding an instantiation is as easy as typing Ctrl+Space. Sigasi Studio marks your syntax errors as you type so you can fix them right away.

**Code browsing_** Sigasi Studio serves as a code browser for VHDL, Verilog and SystemVerilog. You can navigate through your project to understand large and complex legacy designs. Visuals of your code update instantly and are cross-linked to your code to allow graphical browsing.

**Code checking_** See errors while you type and get warnings about dubious code. Save time (and money) as you increase the quality of your VHDL, Verilog or SystemVerilog code. Free up your and your team's valuable time at code reviews to focus on what matters most.

**Documentation_** The Documentation Generator creates an HTML document with all the relevant information from your project. Information will not be duplicated, so it is always consistent and up-to-date.




www.sigasi.com

**FREE TRIAL -** Request your free evaluation today

Date: February 17, 2021

# Sigasi

## FEATURES MATRIX

| | Sigasi Studio XL<br>Our trusted solution for mixed language projects with powerful extra features | Sigasi Studio XPRT<br>Our next generation flagship product with powerful visual feedback tools |
|---|---|---|
| Great code editor | ✔ | ✔ |
| Autocomplete | ✔ | ✔ |
| Syntax validation and Quick Fixes | ✔ | ✔ |
| Format code | ✔ | ✔ |
| Rename refactoring | ✔ | ✔ |
| Find References | ✔ | ✔ |
| Integrates with simulators | ✔ | ✔ |
| Mixed Language (VHDL/Verilog/SystemVerilog) | ✔ | ✔ |
| Preprocessor View for Verilog and SystemVerilog | ✔ | ✔ |
| Supports UVM | ✔ | ✔ |
| Hierarchy View | ✔ | ✔ |
| Offline updates | ✔ | ✔ |
| Integrates with linters | ✔ | ✔ |
| Net Search | ✔ | ✔ |
| Advanced Type Time Linting | ✔ | ✔ |
| VUnit integration | | ✔ |
| Class Hierarchy | | ✔ |
| **Graphical views** | | |
| Compilation Dependencies | ✔ | ✔ |
| Block Diagram | | ✔ |
| State Machine Diagram | | ✔ |
| **Documentation Generation** | | |
| Generate HTML Documentation | | ✔ |

| GRAPHICAL VIEWS | LIVE UPDATE | NAVIGATION | EXPORT | CONFIGURATION |
|---|---|---|---|---|
| State Machine Diagram | Type Time | Linked with source | PNG/SVG | Graphics config file |
| Block Diagram | Type Time | Linked with source | PNG/SVG | Graphics config file |
| Dependencies | Type Time | Linked with source | PNG/SVG | File or Project level |

### DOCUMENTATION GENERATION

| | |
|---|---|
| One-click HTML export | Live preview |
| Markup your documentation with Markdown | Includes Block & FSM diagrams |

ABB THALES NXP HARRIS GE ASML

BOSCH EPSON DOLBY DIGITAL CERN AIRBUS BS

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