TechTalks

Michael Geissel talks with Anupam Bakshi, CEO and Founder of Agnisys

9. AUGUST

eVision Systems
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Angisys and the future of HW-SW Codesign

As a company we as eVision are always looking to new technology that can help our customers to improve their design methodology.

One of the issues that we know from discussions with customers is the consistency of register definitions in HDL and programming languages or in other words the interface between HW and SW. There are currently a lot of individual and hand-crafted solutions in the market which are usually going back to spreadsheets that need to be maintained manually. Actually, it goes beyond registers, into programming sequences around registers and memories.

One of our company founders, Michael Geissel, had recently a discussion with Anupam Bakshi, Agnisys's founder and CEO. Due to Corona, they did their yearly private talk trough a web meeting instead of a private meeting in a pub. They did talk about the reason for automating register design and verification.

> ***" Whatever your methodology might be today, we are sure that we could increase the quality of your design flow with added automation and additional checks in your flow. "***

Anupam, it's great talking to you. One thing that I always wanted to ask you: What was the reason for you to start your company originally?

Since registers are important for a lot of tasks like HDL implementation, SW implementation, HW- and SW test and documentation it is extreme important to make sure that the key data like address definitions and register types are consistent in all models. It appears too often, that inconsistencies are ending up in long debugging sessions or even late detected faults finding their way into the first real chip.

How can Agnisys help?

Since more than a decade we at Agnisys, an innovative EDA company, have focused on exactly this problem. With a comprehensive tool suite offering Editors to enter the register data, code generators to create HDL and SW models from the

specification to verification tools that are allowing to generate automatic test sequences, assertions, properties and UVM models for your test environment.

Why should our customers talk with you?

We are convinced that our technology can help you to improve your design productivity and reduce your design risk. However, we have learned that every company has their own priorities and special requirements. Our solution is very scalable and flexible, and we would like to understand your current methodology. Are you using spreadsheets or are you already using high level models like System-RDL or IP-XACT. Whatever your methodology might be today, we are sure that we could increase the quality of your design flow with added automation and additional checks in your flow.

How are your customers using the technology as of today?

Well, we have seen quite some different use models. Most of our customers are using our software right from the beginning of the system specification. The system Architect uses IDesignSpec, which is a great tool to create a specification of the HW-SW interface without being an expert in Programming languages or HDL languages, since she/he can use a very generic model for nailing down address ranges, register types or register behavior for example.

We have also seen customers that do new ASICs that incorporate a lot of existing models, foreign IP blocks and models from other parts of the company or 3rd parties. In those situations, it is not easy to investigate if those IP modules work smoothly together or if there are overlapping areas of register for example. We can do those checks automatically and simplify their life extremely. Last but not the least, the majority of users are the HDL and SW developers that can use the generated models and that also have the benefit form the generated documentation.

There are a lot of different flows in the market. Some people use spreadsheets, some use IP-XACT and some are using System-RDL. Is there a "golden" approach form your point of view?

Our philosophy is to be as open as possible to support every customer in the best way. Our solutions are compatible with a lot of different input formats. We can support documents from Microsoft Word or Excel, Open Office, IP-XACT or System-RDL. With our product IDS NextGen we have a very unique tool in the market that allows the user to generate not only register implementation models but also complete sequences. Our focus is not to support a specific language but to solve a problem by providing a generic methodology.

Do you see specific advantage of IP-XACT or System-RDL? Would you like to recommend

something to customers or do you really not care?

IP-XACT and SystemRDL are two standards created by Accellera. They both have a specific purpose. While IP-XACT is good as a data interchange format, its not good for data entry. SystemRDL on the other hand is good for data entry, but it lacks the connectivity and architectural features that IP-XACT has. For IDesignSpec it really doesn't matter as it can read in all formats. In fact the tool can read a mix of these and other formats as well.

*When I am talking to customers most engineers need to explain to their management what the benefit of EDA tools are for their company. Would it be appropriate to give a rough number for the return of invest? I mean do your customers have a usual percentage of savings in their design flow*s?

There are two types of savings that are achieved when a customer deploys IDesignSpec product suite:

1. There is the cost saving in terms of the engineering time for architects, designers, verification engineers, firmware, and lab debug etc. Anecdotal evidence suggests this cost saving to be between 20-30%.
2. There is the cost saving in terms of creating a bug free design. The actual saving depends on the product being developed, the penalty for having a bug and it could be anywhere from hundreds of thousands of dollars to over millions of dollars.

Thanks a lot Anupam for your time and I am really looking forward to seeing you face to face when when we have our next meeting.

Anupam Bakshi

Michael Geissel