Agnisys @ DVCon Europe: Showcasing Test Sequence Generator for RISC-V Cores and SoCs

Munich, Germany – October 21, 2019 – Agnisys, Inc., the leading EDA provider of the industry's most comprehensive solution for Design and Verification of SoC Hardware/Software Interface (HSI), to showcase a novel test sequence generator for RISC-V cores and SoCs at DVCon Europe in Munich Germany on October 29-30, 2019.

"One of the main challenges in creating test sequences is that the same sequence functionality must be coded by multiple engineers several times in UVM, C or CSV to support various test environments," said Anupam Bakshi, Founder/CEO. "This aspect of verification can certainly be automated to increase team productivity."

Employing a golden-spec methodology, ISequenceSpec™ provides the environment for describing test sequences in pseudo-code using Python text, Word™ document or Excel™ spreadsheet. The sequence generator is able to re-target the sequences in various languages such as SystemVerilog UVM for simulation, C/Python for firmware tests and Python/C/ASCII/CSV for board testing.

We cordially invite you to see our demo at Booth #301. The demo is based on SweRV™ core, a 32-bit dual-issue 9-stage pipeline open-source processor, where we described the initialization and regular operation sequences for its on-chip Programmable Interrupt Controller. The auto-generated sequences include the following:

UVM Sequence Package for UVM-based Simulation – We create sequence classes that are extended from ‘uvm_reg_sequence’ Arguments are handled here using ‘init´ function. Read/write transactions on registers occurs via register model ‘rm’ inside the task body.

- uvm.sv – sequence file
- uvm.sv – package file

C Sequence Package for Firmware Tests – We create functions with a particular ‘return type’ that can be changed in the configuration settings. Users can perform register and field writes through the tool default APIs or user APIs.

- h – header file
- c – sequence file
- h – API file
- h – package file

Platform Sequence Package for Board Testing – Users can specify the base address of the IP implemented in the board, APIs used for writing/reading the registers, pre-defined initialization and clean up functions . Once generated, the sequences are ready to run on the board.

- h – header file
- c – sequence file

The latest release of ISequenceSpec is now available for download and free evaluation.

Pricing and Availability

Pricing and availability info via email: sales@evision-systems.de

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About ISequenceSpec™

ISequenceSpec provides the environment for capturing the SoC configuration, programming and test sequences in a golden specification. Capture the sequence once in pseudo-code using spreadsheet or text, and generate the required sequences in SystemVerilog for simulation, C/Python for firmware tests, C for emulation and CSV/ASCII for post-silicon validation. Changes in the golden specification only requires re-generation of the target sequence code. With full access to the register and memory map in SystemRDL, IP-XACT or CSV, users can easily capture test sequences for register read/write and transaction-level messages using advanced constructs including loops, if-else, wait, arguments, constant or in-line functions.

About eVision Systems GmbH

eVision Systems GmbH supports companies targeting the development of microelectronics, with a substantial portfolio of measuring- and testing equipment, electronic design automation (EDA) development tools and services.

Since we founded eVision Systems GmbH, it has always been the goal to help young, innovative companies to enter the Central European market. It is common to all their products that the technology is unique, that they are more than an alternative to established solutions and that they enhance and complement existing design flows. Safety in the design, reusability and increased productivity as a result, are the success factors for their customers.

Together with ALDEC, Agnisys, Dediprog, Micron Advanced Computing Solutions, One Spin Solutions, Passmark, PEmicro Computer Systems, Prodigy Technovations, Sigasi and Total Phase, we work with customers throughout Europe.

You can find more information on our website: www.evision-systems.de or on our online shop www.evision-webshop.de.

About Agnisys

Agnisys, Inc. is a leading supplier of Electronic Design Automation (EDA) software for solving complex design and verification problems for system development. Its products provide a common specification-driven development flow to describe registers and sequences for System-on-Chip (SoC) and intellectual property (IP) enabling faster design, verification, firmware, and validation. Based on patented technology and intuitive user interfaces, its products increase productivity and efficiency while eliminating system design and verification errors. Founded in 2007, Agnisys is based in Boston, Massachusetts with R&D centers in the United States and India. www.agnisys.com